IN THE CLAIMS:

Please amend the claims as follows:

1. (original) A method comprising:

receiving a boot block into a secondary location;

pointing an execution address to the secondary location, wherein the execution address is the address from which a processor executes instructions when a system is turned on;

copying the boot block from the secondary location to a primary location; and

pointing the execution address to the primary location.

2. (original) The method of claim 1, pointing an execution address to the secondary location further comprising:

inverting an address bit of the execution address.

3. (original) The method of claim 2, inverting an address bit of the execution address further comprising inverting address bit sixteen of the execution address.

4. (original) The method of claim 1, further comprising:

confirming that the copying of the boot block is complete prior to pointing the execution address to the primary location.

5. (original) The method of claim 1, pointing the execution address to the primary location further comprising de-inverting the address bit of the execution address.

6. (original) A system comprising:

a processor;

a flash memory comprising a primary location and a secondary location; and

a boot block executed from the primary location, wherein the boot block further:

receives a second boot block into the secondary location;

points an execution address to the secondary location;

copies the second boot block to the primary location; and

points the execution address to the primary location.

7. (original) The system of claim 6, further comprising:

an address conversion mechanism for moving the execution address.

8. (original) The system of claim 6, further comprising:

a non-volatile storage for storing the second boot block.

9. (original) The system of claim 6, further comprising:

a network interface card for connecting a system to a network and for downloading the second boot block to the system.

10. (original) The system of claim 6, further comprising:

a backup battery for maintaining the state of an address bit following a power cycle.

11. (original) The system of claim 10, further comprising:

a jumper for adjusting the address bit if the backup battery fails.

12. (original) An article comprising a medium storing instructions for enabling a processor-based system to:

receive a new boot block into a secondary location;

point an execution address to the secondary location, wherein the execution address is the address from which a processor executes instructions when the processor-based system is turned on;

copy the new boot block from the secondary location to a primary location; and

point the execution address to the first location.

13. (original) The article of claim 12, further storing instructions for enabling a processor-based system to:

invert an address bit of the execution address.

14. (original) The article of claim 13, further storing instructions for enabling the processor-based system:

invert address bit sixteen of the execution address.

15. (original) The article of claim 12, further storing instructions for enabling a processor-based system to:

confirm that the copying of the new boot block is complete prior to pointing the execution address to the primary location.

16. (original) The article of claim 12, further storing instructions for enabling a processor-based system to:

de-invert the address bit of the execution address.

17. (currently amended) A method comprising:

copying a boot block from a primary location to a secondary location;

modifying an address bit of ~~pointing~~ an execution address to point to the secondary location, wherein the execution address is the address from which a processor executes instructions when a system is turned on;

maintaining the state of the modified address bit of the execution address following a power cycle;

copying a new boot block to the primary location; and

pointing the execution address to the primary location.

18. (original) The method of claim 17, pointing an execution address to the secondary location further comprising inverting an address bit of the execution address.

19. (original) The method of claim 17, further comprising:

confirming that the copying of the boot block is complete prior to pointing the execution address to the primary location.

20. (currently amended) A system comprising:

a processor;

a flash memory comprising a primary location and a secondary location; and

a boot block executed from the primary location, wherein the boot block further:

is copied to the secondary location;

modifies an address bit of ~~points~~ an execution address to point to the secondary location;

maintains the state of the modified address bit of the execution address following a power cycle;

copies a new boot block to the primary location; and

points the execution address to the primary location.

21. (original) The system of claim 20, further comprising:

an address conversion mechanism for moving the execution address.

22. (original) The system of claim 21, further comprising:

backup battery for maintaining the state of an address bit following a power cycle.

23. (currently amended) The system of claim ~~20~~ 22, further comprising:

a jumper for adjusting the address bit if the backup battery fails.

24. (currently amended) An article comprising a medium storing instructions for enabling a processor-based system to:

copy a boot block from a primary location to a secondary location;

modify an address bit of ~~point~~ an execution address to point to the secondary location, wherein the execution address is the address from which a processor executes instructions when a system is turned on;

maintain the state of the modified address bit of the execution address following a power cycle;

copy a new boot block to the primary location; and

point the execution address to the primary location.

25. (original) The article of claim 24, further storing instructions for enabling a processor-based system to:

confirm that the copying of the boot block is complete prior to pointing the execution address to the primary location.

26. (original) A method comprising:

receiving an upgrade program into a secondary location;

executing instructions from the secondary location by a processor;

copying the upgrade program from the secondary location to a primary location; and

executing instructions from the primary location.

27. (original) The method of claim 26, further comprising:

modifying a logic component such that an execution address is pointed to the secondary location.

28. (original) The method of claim 26, further comprising:

modifying an address bit such that an execution address is pointed to the secondary location.